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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/678,103	10/06/2003	Tsukasa Ooishi	67161-113	1069

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EXAMINER	
DINH, SON T	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 03/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/678,103	OOISHI, TSUKASA	
	Examiner	Art Unit	
	son t dinh	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3 and 4* is/are allowed.

6)☒ Claim(s) *1,2 and 5-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/6/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *East search history*.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 5, 7-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Hidaka (U.S. Patent No 6,635,934).

With respect to claim 1, Hidaka (see figure 19) discloses a memory device having operation modes of a first mode (active mode that includes a normal mode, also see figure 20) and a second mode (standby mode or power down mode, see figure 20), the meomory device comprising a main power supply line (30, figure 19), a sub power supply line (32, figure 19), a first switch (SWa, figure 19) connecting the sub power supply line (32) to the main power supply line (30) in the first mode (active mode, see column 24, lines 50-55) and disconnecting the sub power supply line (32) from the main power supply line (30) in the second mode (see figure 20 and column 24, lines 50-55),

an internal circuit (PQa, PQb, PQc, PQd, NQa, NQb, NQc, NQd) operating according to an input signal (IN, figure 19) in the first mode and entering a standby state in the second mode, the internal circuit including a first field effect transistor (NQa of PQb, or NQc, or PQd) having a gate insulating film with a predetermined thickness (namely Tox1) and kept in a non-conductive state in the second mode (NQa is OFF in the standby that is a second mode, see column 25, lines 6-11), a second field effect transistor (PQa, or NQb, or, PQc, or NQd) connected the main power supply line 30 (one end of transistor PQa is connected to the maim power supply line 30 as shown in figure 10) having a gate insulating film with a thickness (Tox2) greater than the predetermined thickness (Tox1) (see column 25, line 12-13) and kept in conductive state in the second mode (see column 24, lines 60-67).

With respect to claim 5, for the purpose of this rejection, an ITR transistor would be considered as a field effect transistor with a thick gate insulating film as shown by Hidaka in column 65, lines 55-57). Hidaka discloses a memory device having operation modes of self refresh and a normal mode (see column 65, lines 1-10) comprising a memory array of dynamic type (200, figure 80), a first internal circuit (205, figure 77) including at least one field effect transistor of first type (a transistor with thin gate insulating film as defined by Hidaka in column 67, lines 64-67), activates in the normal mode and inactivates in the self refresh mode (column 68, lines 3-30), and a second internal circuit (201 or 202) including at least one field effect transistor of a second type (an ITR transistor that includes in the timer 202 or refresh address counter 201, see column 69, lines 43-49) having a gate insulating film thicker than that of the first field

effect transistor and activated in the self refresh mode (see column 68, lines 52-60, when the timer issues a self refresh signal i.e. the transitors in such timer is ON or activated).

With respect to claims 7 and 8, figure 59A of Hidaka discloses a memory device comprising a signal line (150) precharged to a first potential (Vcc) in a standby state (see figure 59B), a first field effect transistor (NQ17) coupling to the signal line 150 to a second potential (ground, as shown in figure 59A), a second field effect transistor (PTR15) coupling the signal line 150 to the first potential (Vcc) in the standby state. Note that the transistor NQ17 has a thin gate insulating film (column 56, lines 52-53) and transistor PTR15 is an ITR transistor (transistor with thick gate insulating film as explained above). Also, the signal line 150 is a data line between a DRAM (storage data) and any external circuit (like a decoder, or peripheral circuit).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hidaka in view of Arimoto (U.S. Patent No 6,256,252).

Hidaka applied as above. Further, the reference of Hidaka clearly shows that a standby mode (power down mode) and an acive mode (normal mode). The difference

between Hidaka and claims 2 and 6 is that Hidaka is silent on the use of switch connected between a power supply and power supply line (any line that supply power to the device) so as to disconnect the power supply from the memory device in a deep power down mode (or sleep mode).

Arimoto (see figure 23) teaches that the use of a switch between a power supply (namely VDDM) and power supply line (the line between SWm and memory 80 in figure 23) so as to disconnect the power supply node from the power supply line in a sleep mode (or deep power down mode) for the purpose of reducing power consumption is well known in the memory art. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hidaka by incorporating a switch between a power supply node and a power supply line in order to disconnect the power supply node from the power supply line for the purpose of reducing power consumption as taught by Arimoto.

Allowable Subject Matter

Claims 3-4 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fail to teach or suggest a memory device comprising a first internal circuit provided with a power supply potential in a first mode and a second mode, a second internal circuit activated in the first mode and including at least one field effect transistor of a first type, a transmission gate connecting an output of the second

internal circuit to an input node of the first internal circuit in a the first mode and disconnecting the output from the input node in the second mode, and including a field effect transistor of a second type having a gate insulating film thicker than that of the field effect transistor of the first type, and a third internal circuit including at least one field effect transistor of the second type, activated in the second mode and driving the input node.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

-Hidaka (U.S. Patent No 6,487,136) disclose a memory device having self refresh circuit and a precharge circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son Dinh whose telephone number is 571-272-1868. The examiner can normally be reached on 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-1868.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

S. Dinh
March 8, 2005

Son T. Dinh
Primary Examiner